WHAT IS CLAIMED IS:

1. A pulse output circuit comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and second transistors;

a second signal input portion electrically connected to the first electrode of the first transistor;

a third signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type, and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

2. A pulse output circuit comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and

second transistors;

an input change circuit electrically connected to the first electrode of the first transistor;

second and third signal input portions electrically connected to the input change circuit;

a fourth signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type, and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

3. A pulse output circuit comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and second transistors;

an input change circuit electrically connected to the first electrode of the first transistor;

second and third signal input portions electrically connected to the input change

circuit;

a fourth signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type,

wherein the input change circuit is in a first state, conduction is provided between the first electrode of the first transistor and the second signal input section and no conduction is provided between the first electrode of the first transistor and the third signal input section, and

wherein the input change circuit is in a second state, conduction is provided between the first electrode of the first transistor and the third signal input section and no conduction is provided between the first electrode of the first transistor and the second signal input section, and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

4. A pulse output circuit according to claim 2, wherein the input change circuit comprises:

a fourth transistor having a gate electrode, first and second electrodes, the first electrode of the fourth transistor electrically connected to the second signal input portion and the second electrode of the fourth transistor electrically connected to the first electrode of the

first transistor;

a fifth transistor having a gate electrode, first and second electrodes, the first electrode of the fifth transistor electrically connected to the third signal input portion and the second electrode of the fifth transistor electrically connected to the first electrode of the first transistor;

a fifth signal input portion electrically connected to the gate electrode of the fourth transistor; and

a sixth signal input portion electrically connected to the gate electrode of the fifth transistor,

wherein the fourth and fifth transistors are the same conductivity type;

wherein an input change signal is input to said fifth signal input section, and when an inverted input change signal is input to said sixth signal input section, said fourth transistor is set in a conducting state and said fifth transistor is set in a nonconducting state; and

wherein the polarity of the input change signal is reversed, and when the polarity of the inverted input change signal is reversed, said fourth transistor is set in a nonconducting state and said fifth transistor is set in a conducting state.

5. A pulse output circuit according to claim 3, wherein the input change circuit comprises:

a fourth transistor having a gate electrode, first and second electrodes, the first electrode of the fourth transistor electrically connected to the second signal input portion and the second electrode of the fourth transistor electrically connected to the first electrode of the first transistor;

a fifth transistor having a gate electrode, first and second electrodes, the first

electrode of the fifth transistor electrically connected to the third signal input portion and the second electrode of the fifth transistor electrically connected to the first electrode of the first transistor;

a fifth signal input portion electrically connected to the gate electrode of the fourth transistor; and

a sixth signal input portion electrically connected to the gate electrode of the fifth transistor,

wherein the fourth and fifth transistors are the same conductivity type;

wherein an input change signal is input to said fifth signal input section, and when an inverted input change signal is input to said sixth signal input section, said fourth transistor is set in a conducting state and said fifth transistor is set in a nonconducting state; and

wherein the polarity of the input change signal is reversed, and when the polarity of the inverted input change signal is reversed, said fourth transistor is set in a nonconducting state and said fifth transistor is set in a conducting state.

6. A pulse output circuit according to claim 1, wherein said capacitor means is formed between the gate electrode of said second transistor and an active layer of said second transistor.

7. —A pulse output circuit according to claim 2, wherein said capacitor means is formed between the gate electrode of said second transistor and an active layer of said second transistor.

8. A pulse output circuit according to claim 3, wherein said capacitor means is

formed between the gate electrode of said second transistor and an active layer of said second transistor.

9. A pulse output circuit according to claim 1, wherein said capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

10. A pulse output circuit according to claim 2, wherein said capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

11. A pulse output circuit according to claim 3, wherein said capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

12. A shift register comprising a plurality of stages each formed by the pulse output circuit as set forth in claim 1,

wherein sampling pulses are successively output on the basis of first to fourth clock signals and a start pulse.

13. A shift register comprising a plurality of stages each formed by the pulse output circuit as set forth in claim 2,

wherein sampling pulses are successively output on the basis of first to fourth clock signals and a start pulse.

14. A shift register comprising a plurality of stages each formed by the pulse output circuit as set forth in claim 3,

wherein sampling pulses are successively output on the basis of first to fourth clock signals and a start pulse.

15. A shift register comprising a plurality of stages each formed by the pulse output circuit as set forth in claim 1,

wherein the shift register comprises first to fourth clock signal lines and a start pulse input line;

wherein, in said pulse output circuit forming the (4n-3) th stage (n: a natural number, $1 \leq n$), said first signal input section is electrically connected to said first clock signal line;

said second signal input section is electrically connected to said start pulse input line if $n = 1$, or to said signal output section of said pulse output circuit forming the (4n-1) th stage if $n \neq 1$; and

said third signal input section is electrically connected to said third clock signal line;

wherein, in said pulse output circuit forming the (4n-2) th stage, said first signal input section is electrically connected to said second clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-3) th stage; and

said third signal input section is electrically connected to said fourth clock signal line;

wherein, in said pulse output circuit forming the (4n-1) th stage, said first signal input section is electrically connected to said third clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-2) th stage; and

said third signal input section is electrically connected to said first clock signal line;

wherein, in said pulse output circuit forming the 4n th stage, said first signal input section is electrically connected to said fourth clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-1) th stage; and

said third signal input section is electrically connected to said second clock signal line; and

wherein sampling pulses are successively output on the basis of first to fourth clock signals and a start pulse.

16. A shift register comprising:

a plurality of stages each formed by the pulse output circuit according to claim 2; and

first to fourth clock signal lines and a start pulse input line,

wherein, in said pulse output circuit forming the (4n-3) th stage (n: a natural number, $1 \leq n$), said first signal input section is electrically connected to said first clock signal line;

said second signal input section is electrically connected to said start pulse input line if $n = 1$, or to said signal output section of said pulse output circuit forming the (4n-1) th stage if $n \neq 1$;

said third signal input section is electrically connected to one of said start pulse input line and said signal output section of said pulse output circuit forming the (4n-2) th stage; and

said fourth signal input section is electrically connected to said third clock signal

line;

wherein, in said pulse output circuit forming the (4n-2) th stage, said first signal input section is electrically connected to said second clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-3) th stage;

said third signal input section is electrically connected to one of said start pulse input line and said signal output section of said pulse output circuit forming the (4n-1) th stage; and

said fourth signal input section is electrically connected to said fourth clock signal line;

wherein, in said pulse output circuit forming the (4n-1) th stage, said first signal input section is electrically connected to said third clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-2) th stage;

said third signal input section is electrically connected to one of said start pulse input line and said signal output section of said pulse output circuit forming the 4n th stage; and

said fourth signal input section is electrically connected to said first clock signal line;

wherein, in said pulse output circuit forming the 4n th stage, said first signal input section is electrically connected to said fourth clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-1) th stage;

said third signal input section is electrically connected to one of said start pulse input line and said signal output section of said pulse output circuit forming the (4n+1) th stage; and

said fourth signal input section is electrically connected to said second clock signal line; and

wherein sampling pulses are successively output on the basis of first to fourth clock signals and a start pulse.

17. A shift register comprising:

a plurality of stages each formed by the pulse output circuit according to claim 3; and

first to fourth clock signal lines and a start pulse input line,

wherein, in said pulse output circuit forming the (4n-3) th stage (n: a natural number, $1 \leq n$), said first signal input section is electrically connected to said first clock signal line;

said second signal input section is electrically connected to said start pulse input line if $n = 1$, or to said signal output section of said pulse output circuit forming the (4n-1) th stage if $n \neq 1$;

said third signal input section is electrically connected to one of said start pulse input line and said signal output section of said pulse output circuit forming the (4n-2) th stage; and

said fourth signal input section is electrically connected to said third clock signal line;

wherein, in said pulse output circuit forming the (4n-2) th stage, said first signal input section is electrically connected to said second clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-3) th stage;

said third signal input section is electrically connected to one of said start pulse input line and said signal output section of said pulse output circuit forming the (4n-1) th stage; and

said fourth signal input section is electrically connected to said fourth clock signal line;

wherein, in said pulse output circuit forming the (4n-1) th stage, said first signal input section is electrically connected to said third clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-2) th stage;

said third signal input section is electrically connected to one of said start pulse input line and said signal output section of said pulse output circuit forming the 4n th stage; and

said fourth signal input section is electrically connected to said first clock signal line;

wherein, in said pulse output circuit forming the 4n th stage, said first signal input section is electrically connected to said fourth clock signal line;

said second signal input section is electrically connected to said signal output section of said pulse output circuit forming the (4n-1) th stage;

said third signal input section is electrically connected to one of said start pulse input line and said signal output section of said pulse output circuit forming the (4n+1) th stage; and

said fourth signal input section is electrically connected to said second clock signal line; and

wherein sampling pulses are successively output on the basis of first to fourth clock signals and a start pulse.

18. A pulse output circuit according to claim 1, wherein the conductivity type is an n-channel type.

19. A pulse output circuit according to claim 2, wherein the conductivity type is an n-channel type.

20. A pulse output circuit according to claim 3, wherein the conductivity type is

an n-channel type.

21. A pulse output circuit according to claim 1, wherein the conductivity type is a p-channel type.

22. A pulse output circuit according to claim 2, wherein the conductivity type is a p-channel type.

23. A pulse output circuit according to claim 3, wherein the conductivity type is a p-channel type.

24. A shift register comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and second transistors;

a second signal input portion electrically connected to the first electrode of the first transistor;

a third signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type, and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

25. A shift register comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and second transistors;

an input change circuit electrically connected to the first electrode of the first transistor;

second and third signal input portions electrically connected to the input change circuit;

a fourth signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type, and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

26. A shift register comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and second transistors;

an input change circuit electrically connected to the first electrode of the first transistor;

second and third signal input portions electrically connected to the input change circuit;

a fourth signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type,

wherein the input change circuit is in a first state, conduction is provided between the first electrode of the first transistor and the second signal input section and no conduction is provided between the first electrode of the first transistor and the third signal input section, and

wherein the input change circuit is in a second state, conduction is provided between the first electrode of the first transistor and the third signal input section and no conduction is provided between the first electrode of the first transistor and the second signal input section,

and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

27. A display device comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and second transistors;

a second signal input portion electrically connected to the first electrode of the first transistor;

a third signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type, and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

28. A display device comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and second transistors;

an input change circuit electrically connected to the first electrode of the first transistor;

second and third signal input portions electrically connected to the input change circuit;

a fourth signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type, and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

29. A display device comprising:

first, second and third transistors, each having a gate electrode, a first electrode and a second electrode, and the second electrode of the first transistor electrically connected to the gate electrode of the second transistor;

a first signal input portion electrically connected to the gate electrodes of first and

second transistors;

an input change circuit electrically connected to the first electrode of the first transistor;

second and third signal input portions electrically connected to the input change circuit;

a fourth signal input portion electrically connected to the first electrode of the second transistor;

a power supply electrically connected to the first electrode of the third transistor; and

a signal output portion electrically connected to the second electrodes of the second and third transistors,

wherein the first, second and third transistors are the same conductivity type,

wherein the input change circuit is in a first state, conduction is provided between the first electrode of the first transistor and the second signal input section and no conduction is provided between the first electrode of the first transistor and the third signal input section, and

wherein the input change circuit is in a second state, conduction is provided between the first electrode of the first transistor and the third signal input section and no conduction is provided between the first electrode of the first transistor and the second signal input section, and

wherein capacitor means is disposed between the gate electrode and the first electrode of said second transistor or between the gate electrode and the second electrode of said second transistor.

30. A shift register according to claim 24, wherein the conductivity type is an n-

channel type.

31. A shift register according to claim 25, wherein the conductivity type is an n-channel type.

32. A shift register according to claim 26, wherein the conductivity type is an n-channel type.

33. A display device according to claim 27, wherein the conductivity type is an n-channel type.

34. A display device according to claim 28, wherein the conductivity type is an n-channel type.

35. A display device according to claim 29, wherein the conductivity type is an n-channel type.

36. A shift register according to claim 24, wherein the conductivity type is a p-channel type.

37. A shift register according to claim 25, wherein the conductivity type is a p-channel type.

38. A shift register according to claim 26, wherein the conductivity type is a p-

channel type.

39. A display device according to claim 27, wherein the conductivity type is a p-channel type.

40. A display device according to claim 28, wherein the conductivity type is a p-channel type.

41. A display device according to claim 29, wherein the conductivity type is a p-channel type.

42. A shift register according to claim 24, wherein the capacitor means is formed between the gate electrode of the second transistor and an active layer of the second transistor.

43. A shift register according to claim 25, wherein the capacitor means is formed between the gate electrode of the second transistor and an active layer of the second transistor.

44. A shift register according to claim 26, wherein the capacitor means is formed between the gate electrode of the second transistor and an active layer of the second transistor.

45. A display device according to claim 27, wherein the capacitor means is formed between the gate electrode of the second transistor and an active layer of the second transistor.

46. A display device according to claim 28, wherein the capacitor means is formed

between the gate electrode of the second transistor and an active layer of the second transistor.

47. A display device according to claim 29, wherein the capacitor means is formed between the gate electrode of the second transistor and an active layer of the second transistor.

48. A shift register according to claim 24, wherein the capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

49. A shift register according to claim 25, wherein the capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

50. A shift register according to claim 26, wherein the capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

51. A display device according to claim 27, wherein the capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

52. A display device according to claim 28, wherein the capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

53. A display device according to claim 29, wherein the capacitor means is formed between any two of an active layer material, a material forming the gate electrode, and a wiring material.

54. A display device according to claim 27, wherein the display device is applied in an electronic device selected from the group consisting of a liquid crystal display device, a video camera, a notebook-type personal computer, a portable information terminal, an audio reproduction device, a digital camera and a portable telephone.

55. A display device according to claim 28, wherein the display device is applied in an electronic device selected from the group consisting of a liquid crystal display device, a video camera, a notebook-type personal computer, a portable information terminal, an audio reproduction device, a digital camera and a portable telephone.

56. A display device according to claim 29, wherein the display device is applied in an electronic device selected from the group consisting of a liquid crystal display device, a video camera, a notebook-type personal computer, a portable information terminal, an audio reproduction device, a digital camera and a portable telephone.